Q.P. Code: 16EC431 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech IV Year I Semester Supplementary Examinations November-2020

VLSI DESIGN

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	With neat diagrams, explain the different steps in n-well fabrication of CMOS transistor.	**7M**
	b	State why NMOS technology is preferred more than PMOS technology.	**5M**
		OR	
2	**a**	With neat diagrams, discuss nMOS fabrication process steps.	**6M**
	b	Mention the differences between CMOS and BiCMOS technologies.	**6M**
		UNIT-II	
3	**a**	Explain design rules for wires and MOS transistors.	**6M**
	b	Explain how the p-MOS transistor forms in lambda-based design rules.	**6M**
		OR	
4	**a**	Draw the stick diagram for the following using CMOS logic. (i) $Y=(A+B+C)^I$ (ii) 2-input Nand gate	**6M**
	b	Discuss the different contact cuts with an example to each.	**6M**
		UNIT-III	
5	**a**	Write short notes on (i) Domino CMOS logic. (ii) Floor planning.	**6M**
	b	Explain in detail about DCV logic.	**6M**
		OR	
6	**a**	Explain (i) Power delay estimation. (ii) Pass transistors and transmission gate.	**6M**
	b	Explain how the clock and power distributions employed in VLSI design circuits with diagrams.	**6M**
		UNIT-IV	
7	**a**	List the advantages of Zero/one detector.	**5M**
	b	Draw and explain the shifter implemented by using full adder.	**7M**
		OR	
8	**a**	Write a architecture for a 4- bit Counter in sub circuit design.	**6M**
	b	Explain the 6 transistor Static memory cell.	**6M**
		UNIT-V	
9	**a**	Discuss the merits of FPGA over other architectures.	**6M**
	b	Explain the stuck at 1 and stuck 0 faults with suitable diagrams.	**6M**
		OR	
10	**a**	What is the need for testing? Explain about Fault simulation.	**6M**
	b	Discuss in details about CPLD structure and explain each block.	**6M**

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